Preliminary

Ver 0.1

TFT LCD Specification

Model NO.: TD035STEE1

Customer Signature
Date

Table of Contents

Record of Reversion

Rev	Issued Date	Description
0.0	Jun, 10,2005	New
0.1	Jul, 21, 2005	1. Update 2.GENERAL SPECIFICATION: Power consumption (LCD Panel + Driver IC) 2. Update 5.1 Driving TFT LCD Panel and add note in page9: (1) Supply Current (2) Power consumption (3) Add Note 3: Base on VDDIO=3.0V, VDC=3.0V (4) Add Note 4: LCD Panel + Driver IC 3. Update 7.1 Display timing 4. Update 8.Power On/Off Sequence 5. Update Shock (non-operation) of Reliability in page 20 6. Add Command descriptions in page 27

1. FEATURES

The 3.5" LCD module is the Transflective active matrix color TFT LCD module. LTPS (Low Temperature Poly Silicon) TFT technology is used and it's COG design. The LCD module includes touch panel, backlight and TFT LCD panel with minimal external circuits and components required.

2. GENERAL SPECIFICATION

Item		Description	Unit
Display Size (Diagonal)		3.5 inch (8.9cm)	-
Display Type		Transflective	-
Active Area (HxV)		53.28 X 71.04	mm
Number of Dots (HxV)		480 x RGB x 640	dot
Dot Pitch (HxV)		0.074 X 0.222	mm
Color Arrangement		RGB Stripe	-
Color Numbers		262,144 (6 bits)	-
Outline Dimension (HxVxT)		64 X 85 X 4.1(Max 4.4)* W/O FPC	mm
Weight		TBD	g
Power consumption	LCD Panel + Driver IC	95.16 (Typ.)	mW
	Backlight	432 (Typ, I_F= 20mA)	

* Exclude FPC and protrusions.

3. INPUT/OUTPUT TERMINALS

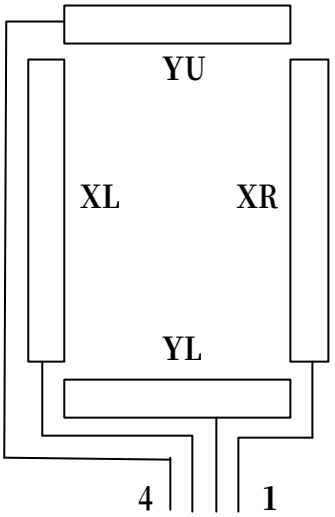
3.1 TFT LCD module

Pin	Symbol	I/O	Description	Remark
1	GND		Digital Ground	
2	YU	I	Y axis position (Top)	
3	XR	I	X axis position (Right)	
4	YL	I	Y axis position (Bottom)	
5	XL	I	X axis position (Left)	
6	GND		Digital Ground	
7	NC		NC	
8	NC		NC	
9	GND		Digital Ground	
10	NC		NC	
11	NC		NC	
12	NC		NC	
13	NC		NC	
14	NC		NC	
15	GND		Digital Ground	
16	NC		NC	
17	XRES	I	Reset Signal	
18	NC		NC	
19	NC		NC	
20	VDC	I	Power supply for booster	
21	GND		Digital Ground	
22	B0	I	Blue Data	
23	B1	I	Blue Data	
24	B2	I	Blue Data	
25	B3	I	Blue Data	
26	B4	I	Blue Data	
27	B5	I	Blue Data	
28	GND		Digital Ground	
29	G0	I	Green Data	
30	G1	I	Green Data	
31	G2	I	Green Data	
32	G3	I	Green Data	
33	G4	I	Green Data	

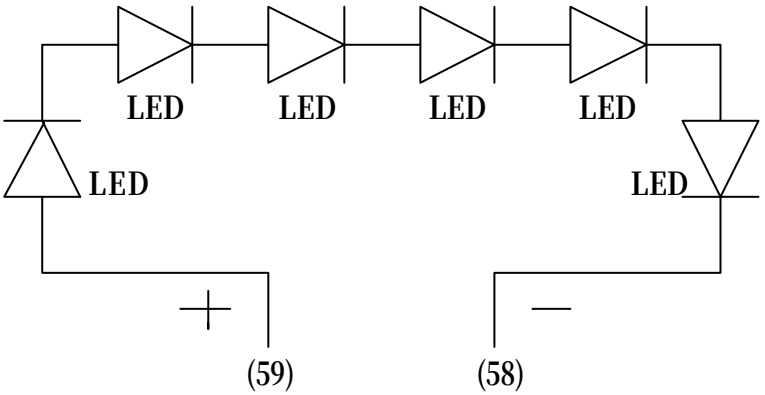
34	G5	I	Green Data	
35	GND		Digital Ground	
36	R0	I	Red Data	
37	R1	I	Red Data	
38	R2	I	Red Data	
39	R3	I	Red Data	
40	R4	I	Red Data	
41	R5	I	Red Data	
42	GND		Digital Ground	
43	VDDIO	I	Logic Supply Voltage	
44	NC		NC	
45	GND		Digital Ground	
46	PCLK	I	Clock signal	
47	GND		Digital Ground	
48	DE	I	Data Enable	
49	DOUT	O	Serial interface data Output	
50	XCS	I	Serial interface chip select	
51	DIN	I	Serial interface data input	
52	NC		NC	
53	SCL	I	Serial interface clock input	
54	VSYNC	I	Vertical SYNC input	
55	HSYNC	I	Horizontal SYNC input	
56	NC		NC	
57	NC		NC	
58	LED-	I	Cathode of LED	
59	LED+	I	Anode of LED	
60	GND		Digital Ground	

3.2 Touch panel Pin

Touch Panel Pin	Module Pin	Symbol	Description	Remark
1	3	XR	Touch Panel Right Side	
2	4	YL	Touch Panel Lower Side	
3	5	XL	Touch Panel Left Side	
4	2	YU	Touch Panel Upper Side	



3.3 Back light pin assignment



4. ABSOLUTE MAXIMUM RATINGS

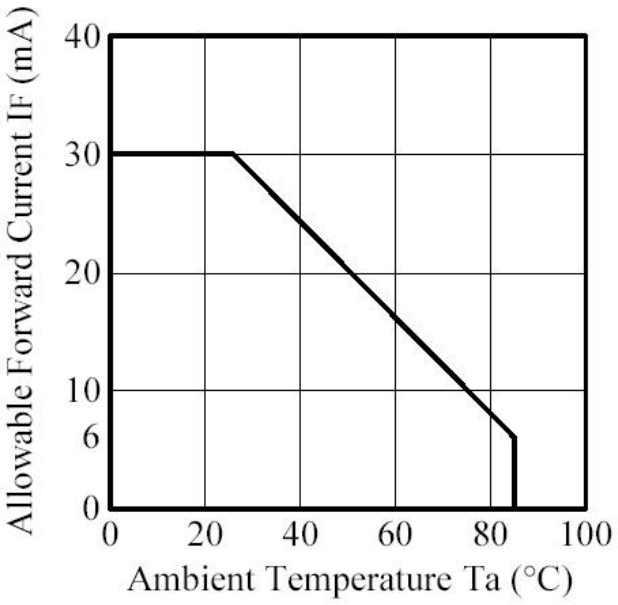
GND=0V

Item	Symbol	MIN	MAX	Unit	Remark
Logic Supply Voltage	VDDIO	-0.3	+6.5	V	
Analog Supply Voltage	VDC	-0.3	+6.5	V	
Maximum supply voltage	V_{IN}	-0.3	VDDIO+0.3	V	
	V_{OUT}	-0.3	VDDIO+0.3	V	
Touch Panel Operation Voltage	V_{Touch}	-	5.0	V	
Backlight LED forward Voltage	V_F	-	4	V	
Backlight LED reverse Voltage	V_R	-	5	V	
Backlight LED forward current (Ta=25℃)	I_F	-	30	mA	Note 2
Operating Temperature	Topr	-10	60	℃	
Storage Temperature	Tstg	-20	70	℃	

Note 1. Reference voltages must satisfy the following relationship: VDC ≧ VDDIO.

Note 2. Relation between maximum LED forward current and ambient temperature is showed as bellow.

■ Ambient Temperature vs.
Allowable Forward Current



5. ELECTRICAL CHARACTERISTICS

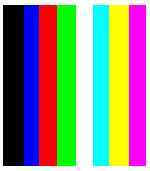
5.1 Driving TFT LCD Panel

Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Supply Voltage	VDDIO	+1.7	+3.0	+3.3	V	
	VDC	+2.7	+3.0	+3.3	V	
Input Voltage	VIL	VSS	–	0.3VDDIO	V	Note 1
	VIH	0.7VDDIO	–	VDDIO	V	
Output Voltage	VOL	VSS	–	0.2VDDIO		DOUT
	VOH	0.8VDDIO	–	VDDIO		
Input Current	I_{IL}	-10	–	–	uA	Note 2
	I_{IH}	–	–	10	uA	
Supply Current	I_{DDIO}	–	0.92	TBD	mA	Note 3
	I_{DC}	–	30.8	TBD	mA	
Power consumption	Power	–	95.16	TBD	mW	Note 4

Note 1: Related pins: VSYNC, HSYNC, DE, PCLK, OSC1, OSC2, FDONIN, XRES, XCS, SCL, DIN, and PD0-17

Note 2: The supply current specification is measured at the line inversion test pattern (Color bar vertical as the diagram shown below).



Note 3: Base on VDDIO=3.0V, VDC=3.0V

Note 4: LCD Panel + Driver IC

5.2 Driving backlight Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	-		30	mA	LED/Part
LED Life Time	-	-	5,000	-	Hr	I_F: 15mA
Forward Current Voltage	V_F	-	(3.6)	4.0	V	I_F: 20mA ,LED/Part

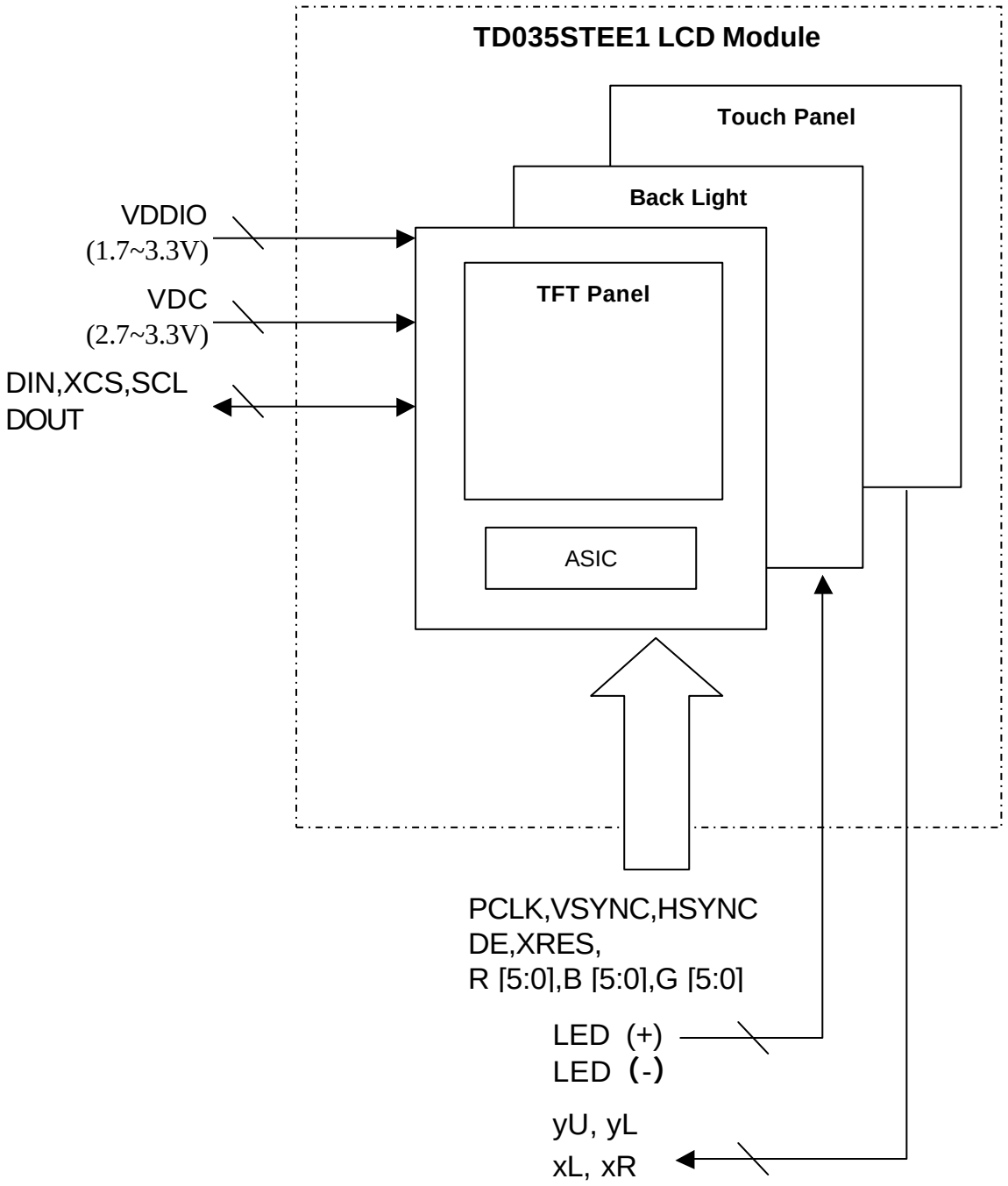
Note: Backlight driving circuit is recommend as the fix current circuit.

5.3 Driving touch panel (Analog resistance type) Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Resistor between terminals (XR-XL)	Rx	100	-	1100	Ω	
Resistor between terminals (YU-YL)	Ry	100	-	1100	Ω	
Operation Voltage	V_{Touch}	-	5.0	-	V	DC
Line Linearity (X direction)	-	-1.5	-	+1.5	%	Note
Line Linearity (Y direction)	-	-1.5	-	+1.5	%	
Chattering	-	-	-	10	ms	
Surface Hardness	-	3	-	-	H	JIS K 5600
Minimum tension for detecting	-	-	-	80	g	
Insulation Resistance	Ri	20	-	-	MΩ	At DC 25V

Note. The minimum test force is 80 g.

6. BLOCK DIAGRAM



7. TIMING CHART

7.1 Display timing

VGA Mode

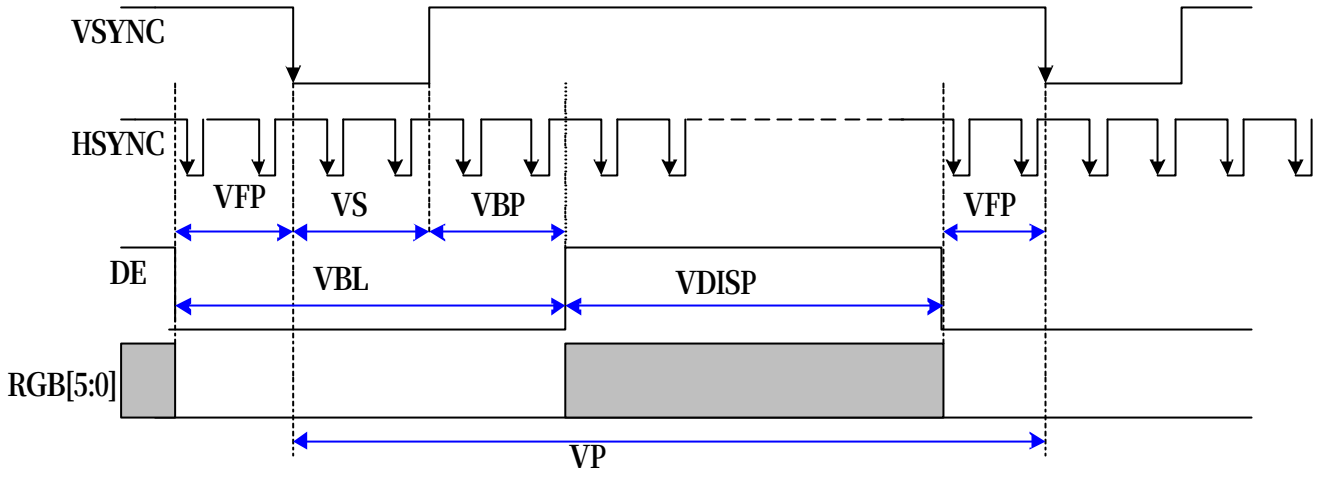
Display Mode	Parameter	Symbol	Conditions	Ratings			Unit
				MIN	TYP	MAX	
Normal	Vertical cycle	VP		646	–	–	Line
	Vertical data start	VDS	VS+VBP	2	–	–	Line
	Vertical Sync Pulse width	VS		2	–	–	Line
	Vertical front porch	VFP		4	–	–	Line
	Vertical Back porch	VBP		0	–	–	Line
	Vertical blanking period	VBL	VS+VBP+VFP	8	–	–	Line
	Vertical active area	VDISP		640	–	–	Line
	Horizontal cycle	HP		520	–	–	dot
	Horizontal front porch	HFP		24	–	–	dot
	Horizontal Sync Pulse width	HS		8	–	–	dot
	Horizontal Back porch	HBP		8	–	–	dot
	Horizontal Data start	HDS	HS+HBP	16	–	–	dot
	Horizontal active area	HDISP		480	–	–	dot
	Clock frequency	tclk		20	TBD	TBD	MHz
		fclk		0.5	TBD	TBD	nS

QVGA Mode

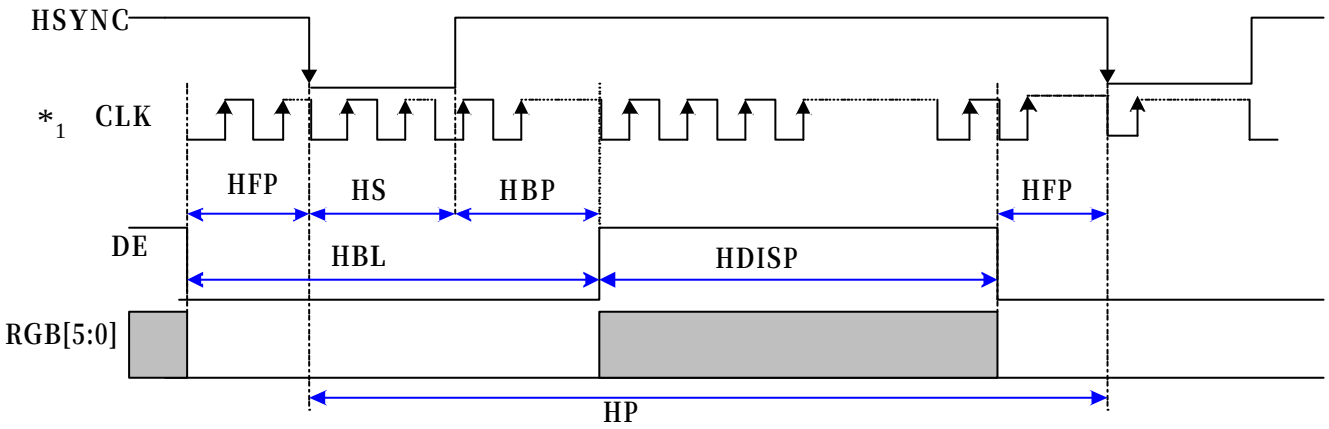
Display Mode	Parameter	Symbol	Conditions	Ratings			Unit
				MIN	TYP	MAX	
Normal	Vertical cycle	VP		326	–	–	Line
	Vertical data start	VDS	VS+VBP	4	–	–	Line
	Vertical Sync Pulse width	VS		2	–	–	Line
	Vertical front porch	VFP		2	–	–	Line
	Vertical Back porch	VBP		2	–	–	Line
	Vertical blanking period	VBL	VS+VBP+VFP	6	–	–	Line
	Vertical active area	VDISP		320	–	–	Line
	Horizontal cycle	HP		344	–	–	dot
	Horizontal front porch	HFP		88	–	–	dot
	Horizontal Sync Pulse width	HS		8	–	–	dot
	Horizontal Back porch	HBP		8	–	–	dot
	Horizontal Data start	HDS	HS+HBP	16	–	–	dot
	Horizontal active area	HDISP		240	–	–	dot
	Clock frequency	tclk		6.5	TBD	TBD	MHz
		fclk		0.015	TBD	TBD	nS

Input timing chart

＜Vertical Timing chart＞

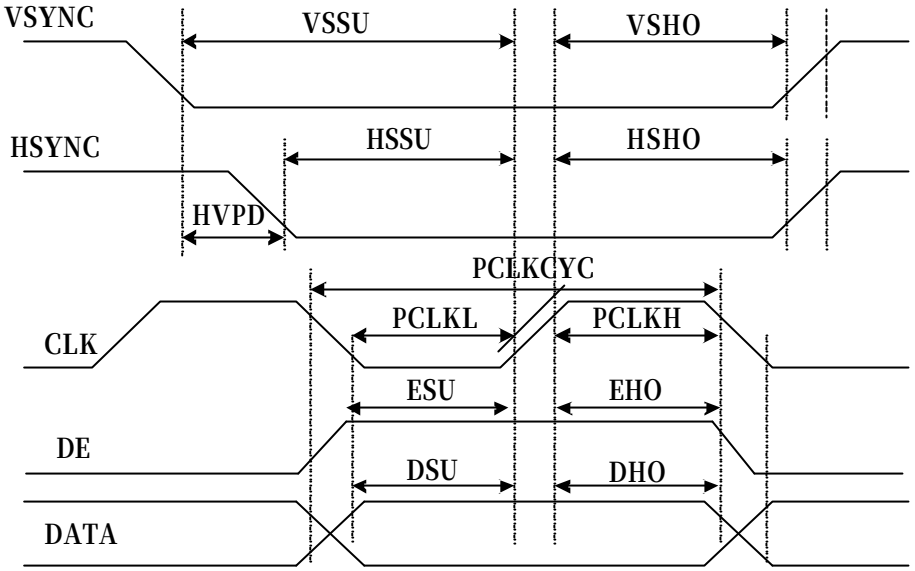


＜Horizontal Timing chart＞



*1. The frequency of CLK should be continued whether in display or blank region to ensure IC operating normally.

Setup/ Hold Timing chart



AC Characteristics:

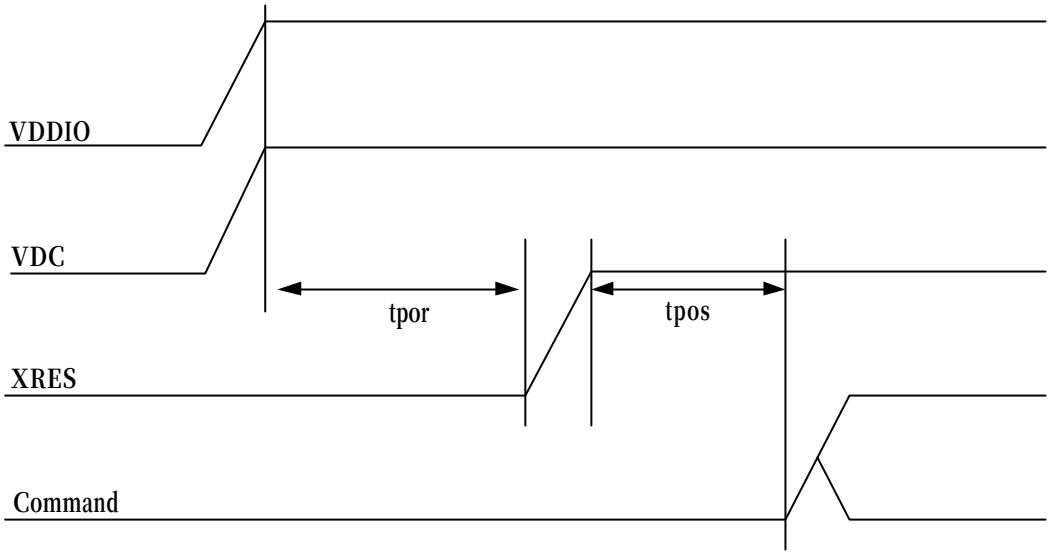
Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
VSYNC Setup time	VSSU		15	–	–	ns
VSYNC Hold time	VSHO		15	–	–	ns
HSYNC Setup time	HSSU		15	–	–	ns
HSYNC Hold time	HSHO		15	–	–	ns
VSYNC-HSYNC Falling edge	HVPD		0	–	–	ns
PCLK cycle time	PCLKCYC		40	–	–	ns
Clock “L” pulse width	PCLKL		20	–	–	ns
Clock “H” pulse width	PCLKH		20	–	–	ns
DE setup time	ESU		15	–	–	ns
DE Hold time	EHO		15	–	–	ns
Data setup time	DSU		15	–	–	ns
Data Hold time	DHO		15	–	–	ns

Note 1：Input signal rise/fall time：tr, tf ≦5 ns

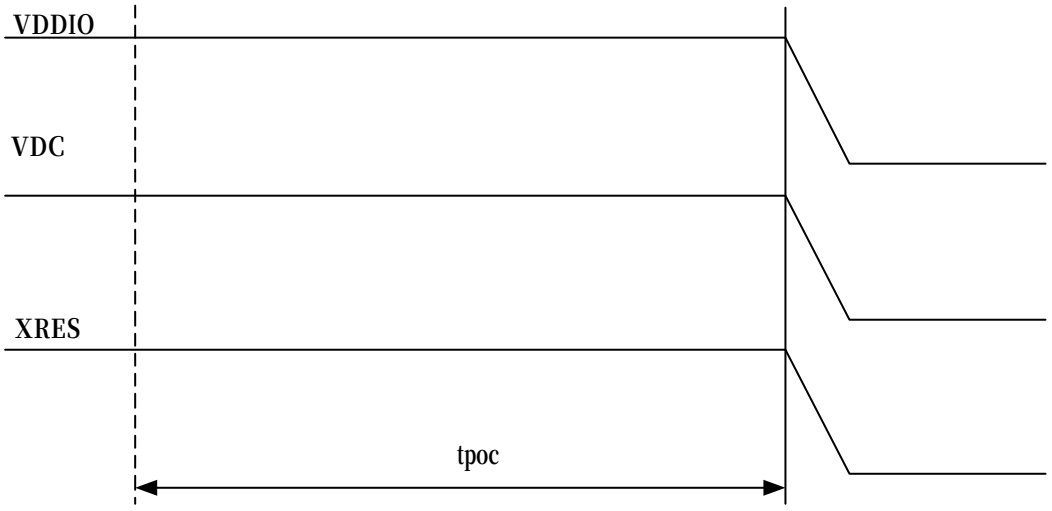
Note 2：The threshold voltage of input signal：VIH = 0.7xVDDIO, VIL = 0.3xVDDIO

8. Power On/Off Sequence

Power on sequence



Power off sequence



Enabled Sleep in command

Characteristics	Symbol	Conditions	Min	Typ.	Max	Unit
Power on reset time	tpor	–	100	–	–	ms
Reset release time	tpos	–	1	–	–	ms
Sleep mode release time	tpoc	–	250	–	–	ms

9. Optical Characteristics

9.1 Optical Specification

(1) Back light Off w / Touch panel

Ta=25℃

Item	Symbol		Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angles	Θ R		CR = 3	TBD	40	-	Degree	Note 9-1
	Θ L			TBD	40	-		
	Θ U			TBD	40	-		
	Θ D			TBD	40	-		
Chromaticity	White	x	Θ =0°	TBD	TBD	TBD	-	Note 9-3
		y		TBD	TBD	TBD	-	
Contrast Ratio	CR		Θ =0°	TBD	8:1	-	-	Note 9-2
Reflectivity	R		Θ =0°	TBD	5	-	%	Note 9-4

(2) Back Light On w / Touch panel

Ta=25℃

Item	Symbol		Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angles	Θ R		CR = 5	TBD	80	-	Degree	Note 9-1
	Θ L			TBD	80	-		
	Θ U			TBD	80	-		
	Θ D			TBD	80	-		
Response Time	Tr+Tf		Θ =0°	-	35	50	ms	Note 9-5
Contrast Ratio	CR		Θ =0°	TBD	180:1	-	-	Note 9-6
Luminance	L		Θ =0° I_F =20mA	TBD	150	-	cd/m^2	Note 9-7
NTSC	-		-	TBD	37	-	%	Note 9-7
Uniformity	-		-	TBD	80	-	%	Note 9-8
Chromaticity	White	x	Θ =0°	TBD	0.31	TBD	-	Note 9-3
		y		TBD	0.33	TBD		

9.2 .Basic measure condition

(1) Driving voltage

VDD= 10.0V, VEE=-5.0V

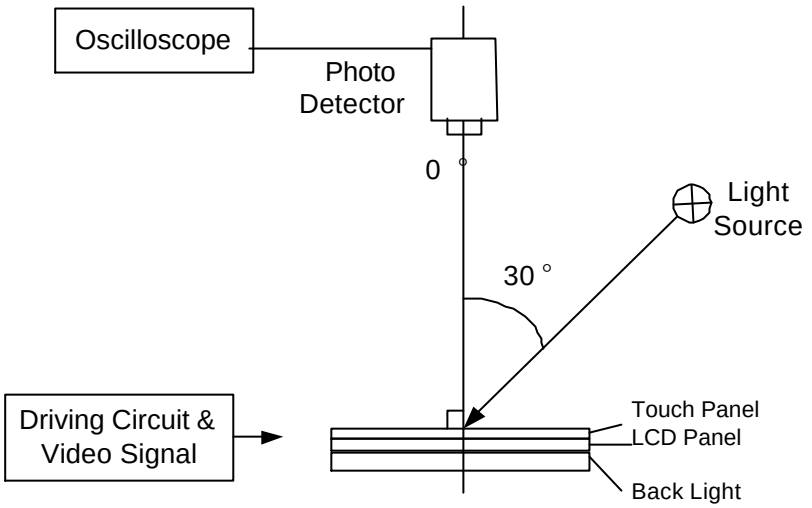
(2) Ambient temperature: Ta=25℃

(3) Testing point: measure in the display center point and the test angle Θ =0 °

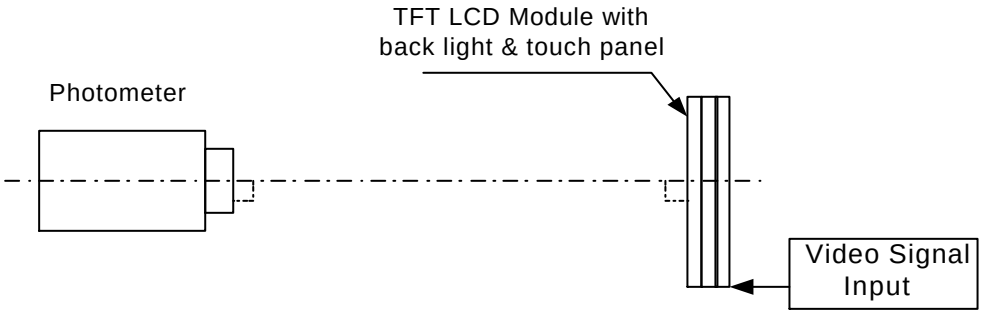
(4) Testing Facility

Environmental illumination: = 1 Lux

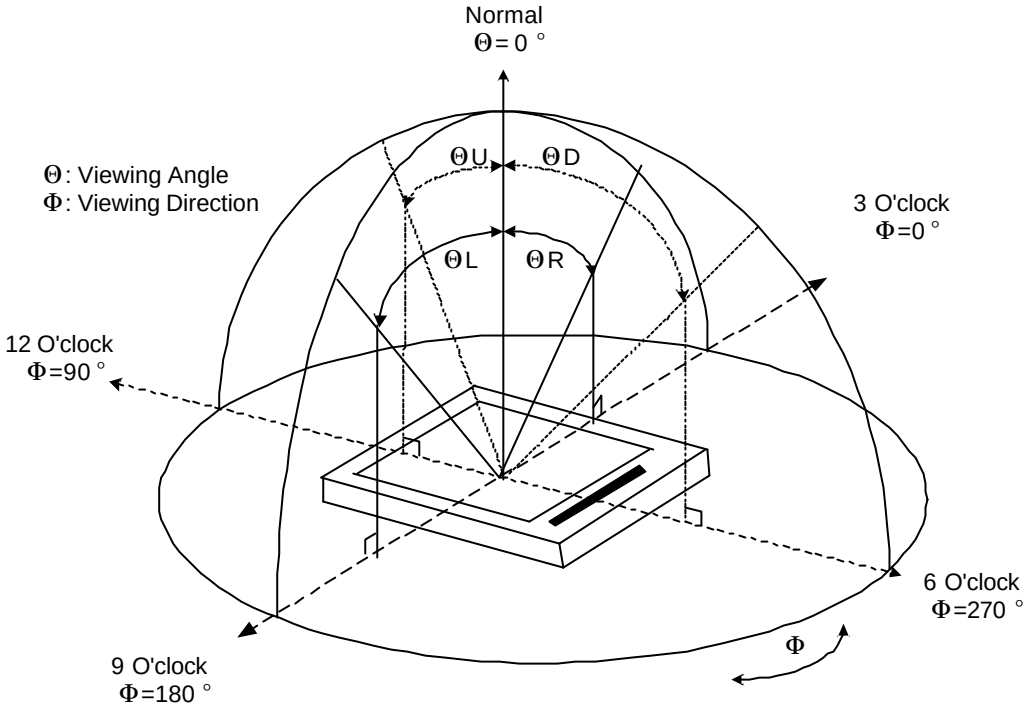
a. System A



b. System B



Note 9-1: Viewing angle diagrams (Measure System A)



Note 9-2: Contrast ratio in back light off (Measure System A)

Contrast Ration is measured in optimum common electrode voltage.

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

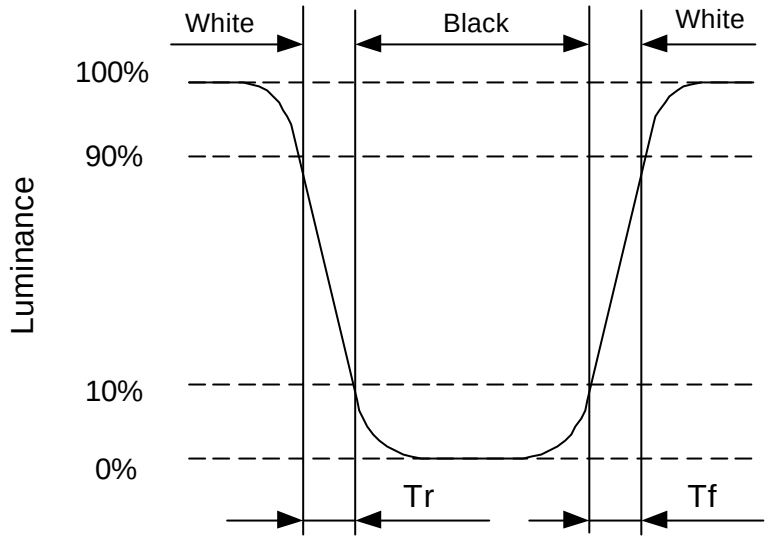
Note 9-3: White chromaticity as back light off: (Measure System A)

Note 9-4: Reflectivity (R) (Measure System A)

In the measuring system A,.calculate the reflectance by the following formula.

$$\text{Reflectivity(R)} = \frac{\text{Output from the white display panel}}{\text{Output from the reflectance standard}} \times \text{Reflectance factor of reflectance standard}$$

Note 9-5: Definition of response time: (Measure System B)



Note 9-6: Contrast Ratio in back light On (Measure System B)

Contrast Ration is measured in optimum common electrode voltage.

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

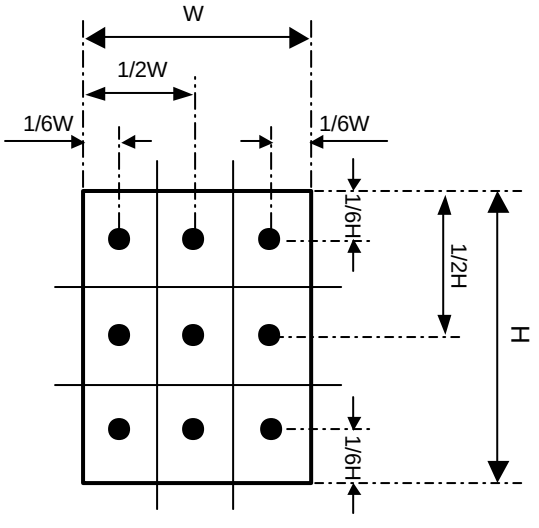
Note 9-7: Luminance: (Measure System B)

Test Point: Display Center

Note 9-8: Uniformity (Measure System B)

The luminance of 9 points as the black dot in the figure shown below are measured and the uniformity is defined as the formula:

$$\text{Uniformity} = \frac{\text{The minimum luminance among 9 points}}{\text{The maximum luminance among 9 points}}$$



Active Area (W x H)

10. Reliability

No	Test Item	Condition
1	High Temperature Operation	Ta=+60℃, 240hrs
2	High Temperature & High Humidity Operation	Ta=+40℃, 95% RH, 240hrs
3	Low Temperature Operation	Ta= -10℃, 240hrs
4	High Temperature Storage (non-operation)	Ta=+70℃, 240hrs
5	Low Temperature Storage (non-operation)	Ta= -20℃, 240hrs
6	Thermal Shock (non-operation)	-20℃(30 min)← → 70℃(30 min),30 cycles
7	Surface Discharge (non-operation) (LCD surface)	C=150pF, R=330 Ω; Discharge: Air: ±15kV; Contact: ±8kV 5 times / Point; 5 Points / Panel
8	Shock (non-operation)	Acceleration: 100G; Period: 2.5 ms Directions: ±X, ±Y, ±Z; Cycles: Three times
9	Pin Activation Test (Touch Panel)	Hit 1,000,000 times with a silicon rubber of R0.8, HS 60. Hitting Force: 250g Hitting Speed: 3 time/sec
10	Writing Friction Resistance Test (Touch Panel)	Pen: 0.8R Polyacetal stylus Load: 250g Speed: 3 Strokes/sec Stroke: 35mm 100000 times

11. Handling Cautions

11.1 ESD (Electrical Static Discharge) strategy

ESD will cause serious damage of the panel, ESD strategy is very important in handling. Following items are the recommended ESD strategy

(1) In handling LCD panel, please wear gloves with non-charged material. Using the conduction ring connect wrist to the earth and the conducting shoes to the earth is necessary.

(2) The machine and working table for the panel should have ESD protection strategy.

(3) In handling the panel, ionized air flowing decrease the charge in the environment is necessary.

(4) In the process of assemble the module; shield case should connect to the ground.

11.2 Environment

(1) Working environment should be clean room.

(2) Because touch panel has protective film on the surface, please remove the protection film slowly with ionized to prevent the electrostatic discharge.

11.3 Touch panel

(1) The front touch panel is vulnerable to heavy weight, so any input must be done by special stylus or by a finger. Do not put any heavy stuff on it.

(2) When any dust or stain is observed on a film surface, clean it using a lens cleaner for glasses or something similar.

11.4 Others

(1) Turn off the power supply before connecting and disconnecting signal input cable.

(2) Because the connection area of FPC and panel is not so strong, do not handle panel only by FPC or bend FPC.

(3) Water drop on the surface when panel is powered on will corrode panel electrode.

(4) Before opening up the packing bag, watch out the environment for the panel storage. High temperature and high humidity environment is prohibited.

(5) In the case the TFT LCD module is broken, please watch out whether liquid crystal leaks out or not. If your hand touches liquid crystal, wash your hands cleanly with water and soap as soon as possible

12. Application Note

12.1 Design notes on touch panel

(1) Explanation of each boundary of touch panel

A. Boundary of Double-sided adhesive

a. Electrically detectable within this zone.

When holding the touch panel by housing, it needs to be held at outside of this zone.

b. Film is supported by double-sided adhesive tape.

B. Viewing area

a. Cosmetic inspection to be done for this area.

This area is set as inside of boundary of double-sided adhesive with tolerance.

C. Boundary of transparent insulation

a. Purpose is to "Help" to secure insulation.

b. Electrical insulation on this area is not guaranteed.

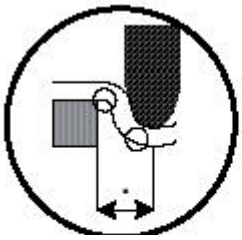
c. We do recommend not to hold this area by something like housing or gasket.

D. Active area

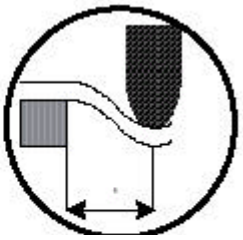
a. This area is where the performance is guaranteed.

This area set as some distance inside from the boundary area of double-sided adhesive tape since its neighboring area is less durable to writing friction.

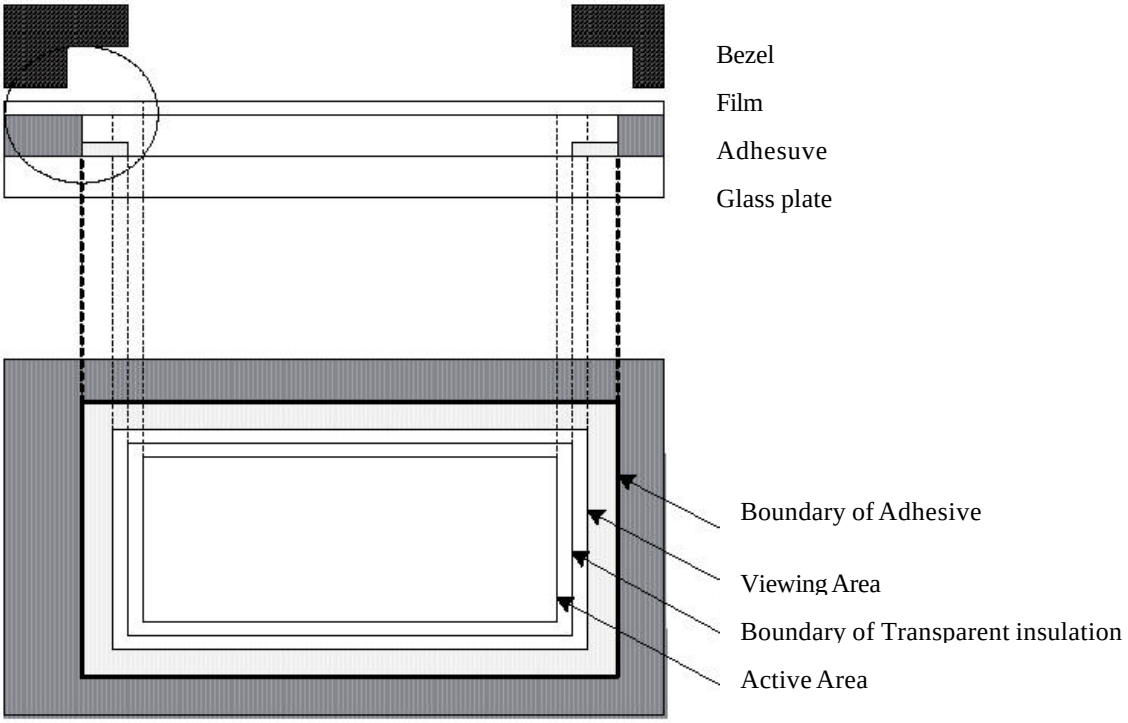
b. Please refer to the attached module drawing for the bezel opening and window size design.



There is some possibility to damage



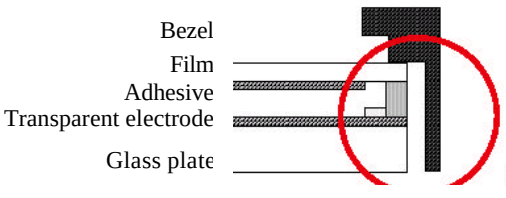
No Damage to ITO



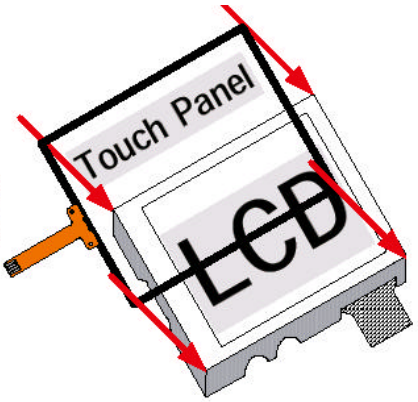
(2) Housing and touch panel

a. Please have clearance between the side of touch panel, and any conductive material such as metal frame.(drawing.1) Transparent electrode exists on glass of touch panel from end to end.

b. It is recommended to fix a touch panel on the LCD module chassis rather than the touch panel housing. Clinging at conductive material and side of touch panel might cause malfunction.



Drawing 1



Drawing 2

12.2 Note for image discharge circuit

(1) The image will remain on display when the power is suddenly cut off in abnormal condition, ie, unit dropped and battery fell out. The phenomenon is because the electrical charge well be held in pixel, if there is no extra input signal to release it, the residual image occurs.

(2) The imaging discharge circuit is used for clearing the image residual on display. The circuit is designed on panel and customer can input signal to driver the function especially in the case that the battery or power supplier unit are removable.

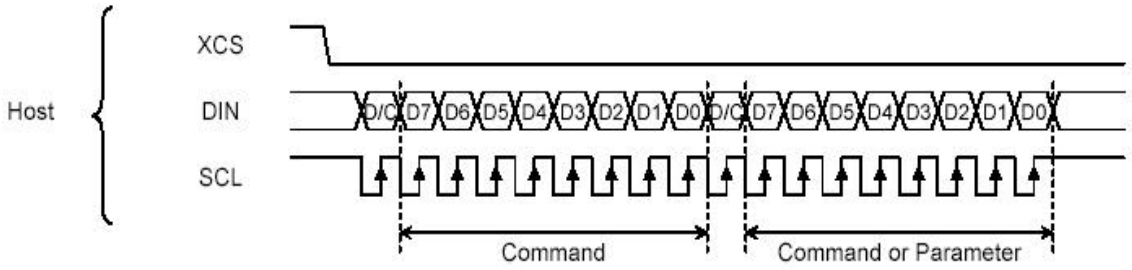
(3) The circuit below is designed on panel to avoid image sticking.

12.3 Note for 3-Wire command

The LCM support the 3-Wire serial interface to set internal register. Read/Write bit D/C, Serial address D7 to D0 (DIN) and serial data D7 to D0 (DOUT) are read at the rising edge of the serial clock, via the serial input pin. This data is synchronized on the rising edge of eighth serial clock and is then converted to parallel data. The serial interface signal timing chart is shown below.

a) Command write instruction

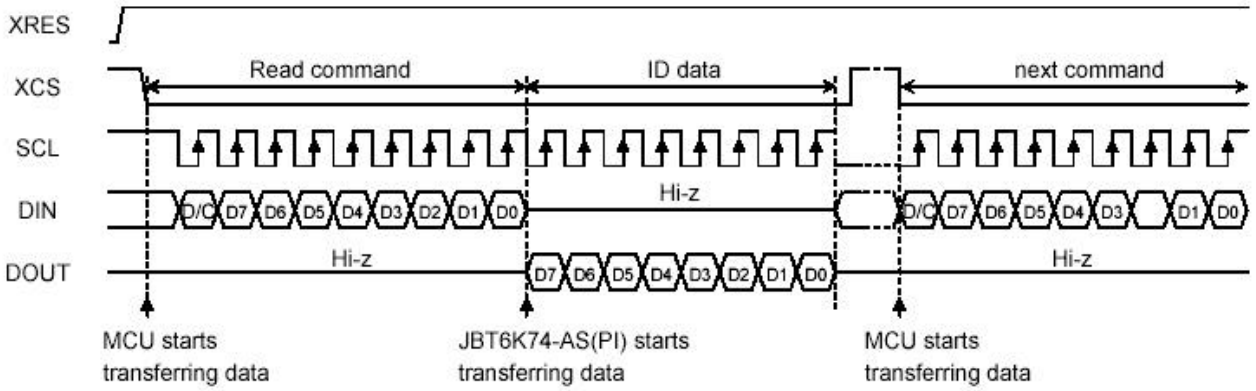
While the XCS signal is low, a zero detected in the DIN signal causes the serial interface controller to recognize the next SCL rising edge as D7 of a command and start fetching data. In the input data, MSB = D7 and LSB = D0. Once the LSB of the command has been input, the serial interface controller expects either a command or parameter data according to the rising edge. If D/C = high, it recognizes the data the host transmits next as a parameter. If D/C = low, it recognizes the next data as a command.



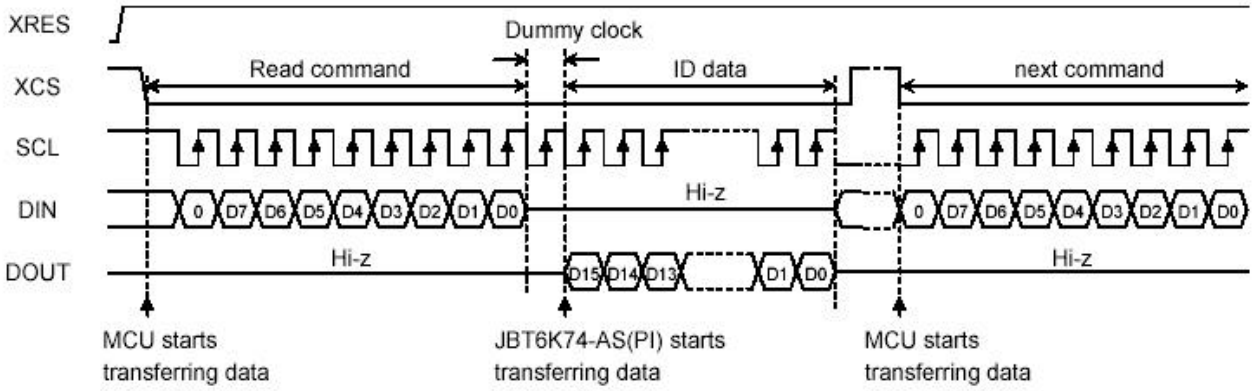
b) Status read

The JBT6K78-AS(PI) allows the host to issue a request (status read instruction) to retrieve the internal chip status and ID information. Status data and ID information are output on the rising edge of SCL. After reading status data and ID information, the host can enable the next command transfer by driving XCS high temporarily and then back low. Note that the status read protocol varies with the operation command type.

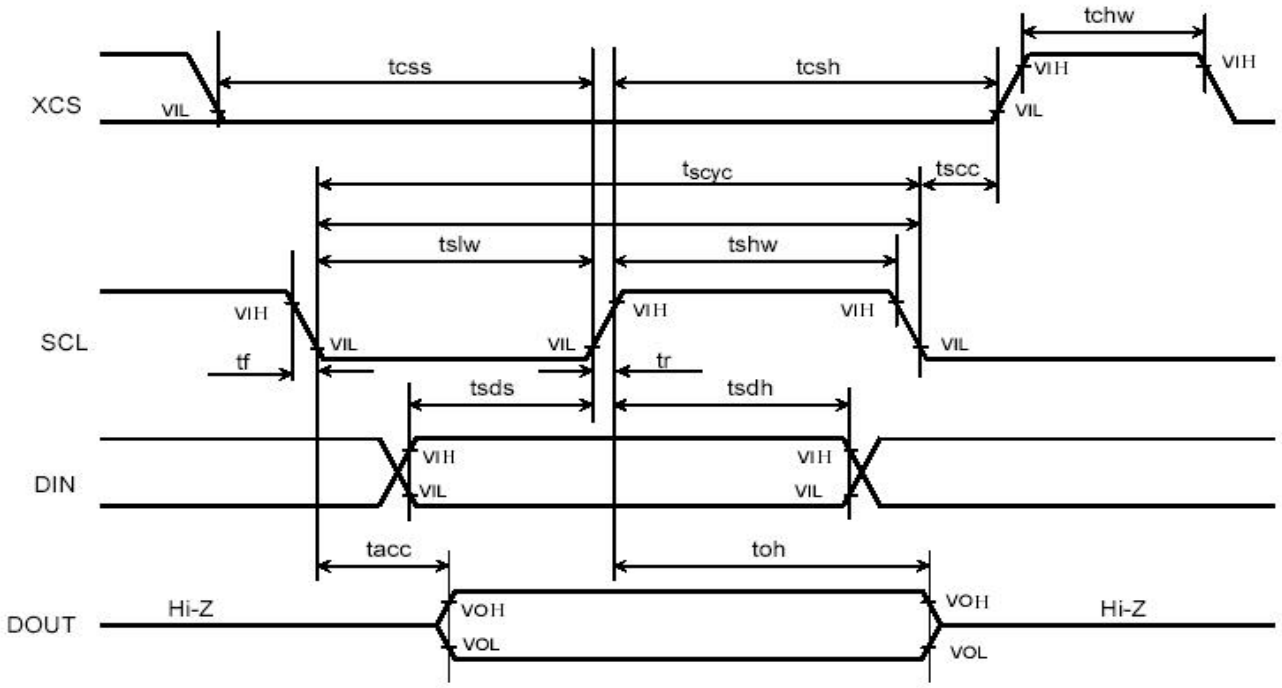
■ For the 8 bits long operation command (06, 07, 08h, and 0Ah to 0Eh)



■ For the 16 or more bits long operation command (04,09h, and EBh)



Serial Interface



Serial interface and Reset							
Parameter		Symbol	Conditions	Min.	Typ.	Max.	Unit
Write mode	Clock cycle	tscyc	∠	100	∠	∠	ns
	SCL “H” Period	tshw	∠	35	∠	∠	ns
	SCL “L” Period	tslw	∠	35	∠	∠	ns
	Data Set-up Time	tsds	∠	20	∠	∠	ns
	Data Hold Time	tsdh	∠	20	∠	∠	ns
Read mode	Clock cycle	tscyc	∠	150	∠	∠	us
	SCL “H” Period	tshw	∠	60	∠	∠	ns
	SCL “L” Period	tslw	∠	60	∠	∠	ns
	Output Data Delay Time	tacc	∠	10	∠	50	ns
	Output Data Hold Time	toh	∠	15	∠	50	ns
XCS “L” cancel time		tscc	∠	20	∠	∠	ns
XCS “H” pulse width		tchw	∠	40	∠	∠	ns
XCS signal setup time		tcss	∠	30	∠	∠	ns
XCS signal hold time		tcsh	∠	35	∠	∠	ns

Note 1：Input signal rise/fall time：tr, tf ≦15 ns

Note 2：The threshold voltage of input signal：VIH = 0.7xVDDIO, VIL = 0.3xVDDIO

Command descriptions：

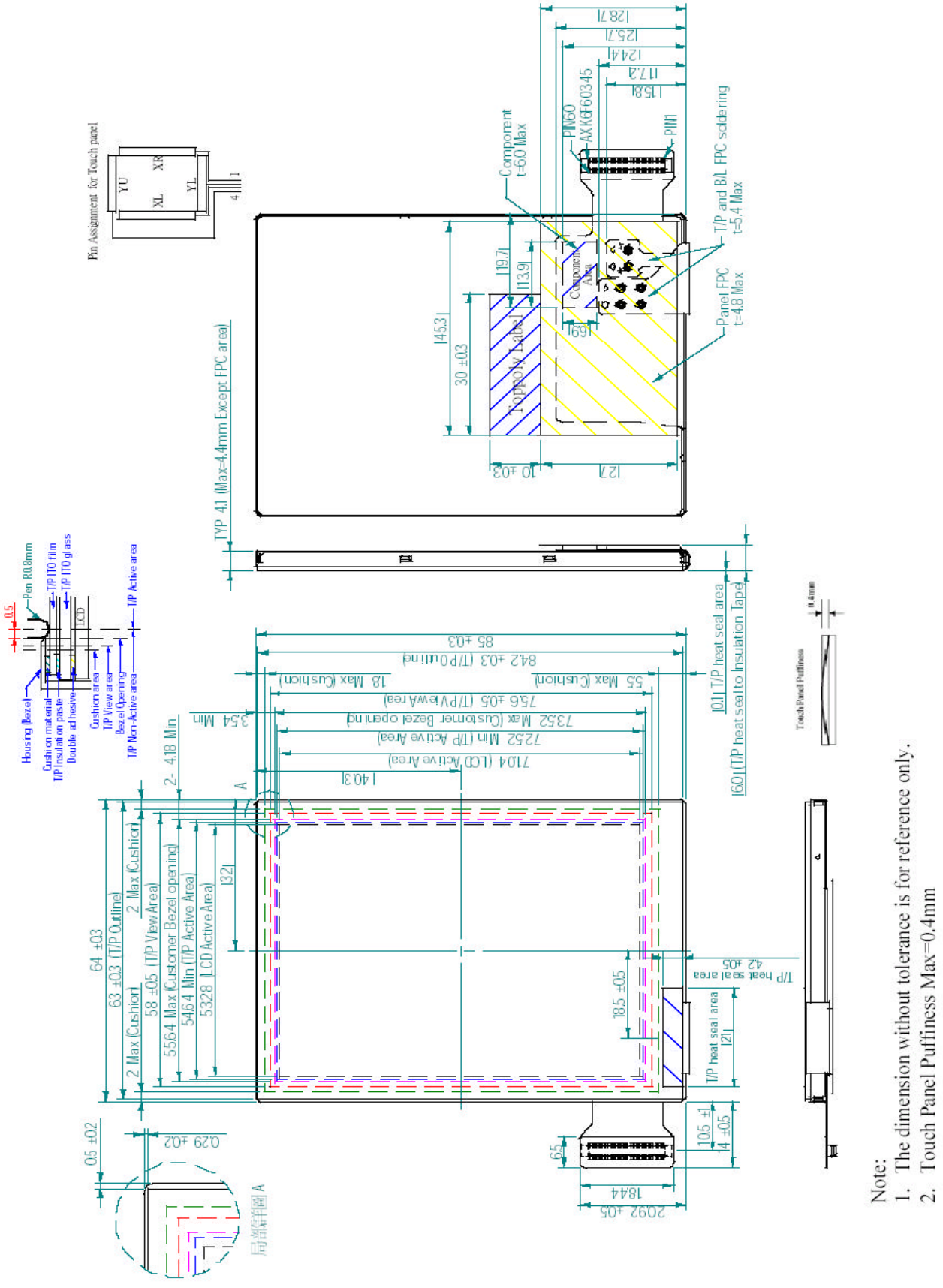
Operation code (hex)	byte	Function	Pin setting			Valid FR sync.mode	R/W/C	Initlal register value [Hex]				1st byte							
			XCS	SCL	XRES			1	2	3	4	D7	D6	D5	D4	D3	D2	D1	D0
Date setup command																			
00	0	No operation	0	+	1		C	-											
01	0	Software rest	0	+	1		C	-											
04	3	Read display identification information	0	+	1		R	74	80	10	00	xx	xx	xx	xx	xx	xx	xx	xx
												0	1	1	1	0	1	0	0
												1	V6	V5	V4	V3	V2	V1	V0
												1	0	0	0	0	0	0	0
												xx	xx	xx	xx	xx	xx	xx	xx
												0	0	0	1	0	0	0	0
06	1	Read red color	0	+	1		R	00	00	00	00	*	*	RCR5	RCR4	RCR3	RCR2	RCR1	RCR0
07	1	Read green color	0	+	1		R	00	00	00	00	*	*	RCG5	RCG4	RCG3	RCG2	RCG1	RCG0
08	1	Read blue color	0	+	1		R	00	00	00	00	*	*	RCB5	RCB4	RCB3	RCB2	RCB1	RCB0
09	4	Read display status	0	+	1		R	00	60	00	00	RDS31	RDS30	RDS29	RDS28	RDS27	RDS26	*	*
												0	0	0	0	0	0	0	0
												*	RDS22	RDS21	RDS20	*	*	RDS17	*
												0	1	1	0	0	0	0	0
												*	*	RDS13	*	*	RDS10	*	*
												0	0	0	0	0	0	0	0
												*	*	*	RDS4	RDS3	RDS2	RDS1	*
												0	0	0	0	0	0	0	0
0A	1	Read display power mode	0	+	1		R	00	00	00	00	RDP7	*	*	RDP4	*	RDP2	*	*
												0	0	0	0	0	0	0	0
0B	1	Read display MADCTL setting	0	+	1		R	00	00	00	00	RDM7	RDM6	RDM5	RDM4	RDM3	*	*	*
												0	0	0	0	0	0	0	0
0C	1	Read interface color format	0	+	1		R	60	00	00	00	*	RDF6	RDF5	RDF4	*	*	*	*
												0	1	1	0	0	0	0	0
0D	1	Read display image mode	0	+	1		R	00	00	00	00	*	*	RDI5	*	*	*	*	*
												0	0	0	0	0	0	0	0
0E	1	Read display signal mode	0	+	1		R	00	00	00	00	*	*	RDS15	RDS14	RDS13	RDS12	*	*
												0	0	0	0	0	0	0	0
10	0	Sleep-in	0	+	1		C	-											
11	0	Sleep-out	0	+	1		C	-											
12	0	Don't use						-											
13	0																		
20	0	Inversion off	0	+	1		C	-											
21	0	Inversion on	0	+	1		C	-											
26		Don't use						00	00	00	00								
28	0	Display off	0	+	1		C	-											
29	0	Display on	0	+	1		C	-											
2A to 30		Don't use						-											
36	1	Memore acceess control	0	+	1		W	00	00	00	00	B7	B6	B5	B4	B3	*	*	*
												0	0	0	0	0	0	0	0
3A	1	RGB lnterface data format	0	+	1		W	60	00	00	00	*	IPF6	IPF5	IPF4	*	*	*	*
												0	1	1	0	0	0	0	0
3B	1	Quad Date configuration	0	+	1		W	00	00	00	00	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
												0	0	0	0	0	0	0	0

Date setup command																			
B0	1	Ppwer supply on/off control	0	+	1		W	16	00	00	00	*	*	*	DSTB	*	AVON	XVON	RVON
												0	0	0	1	0	1	1	0
B1	1	Booster operation setup	0	+	1		W	5A	00	00	00	*	XVV2	XVV1	XVV0	VGAMV3	VGAMV2	VGAMV1	VGAMV0
												0	1	0	1	1	0	1	0
B2	1	Booster mote setup	0	+	1		W	33	00	00	00	*	*	AV23	AVDS	*	*	XV23	XVDS
												0	0	1	1	0	0	1	1
B3	1	Booster frequencies setup	0	+	1		W	11	00	00	00	*	*	FSX1	FSX0	*	*	FSA1	FSA0
												0	0	0	1	0	0	0	1
B4	1	Operational amplifer capability / System clock freq. Division setup	0	+	1		W	01	00	00	00	*	*	SSCLK1	SSCLK0	*	*	ABSW1	ABSW0
												0	0	0	0	0	0	0	1
B5	1	VSC voltage adustment	0	+	1		W	20	00	00	00	*	*	CASJ5	CASJ4	CASJ3	CASJ2	CASJ1	CASJ0
												0	0	1	0	0	0	0	0
B6	1	VCOM voltagee adustment	0	+	1		W	40	00	00	00	*	COMAJ5	COMAJ4	COMAJ3	COMAJ2	COMAJ1	COMAJ0	COMAJ1
												0	1	0	0	0	0	0	0
B7	1	Comfigure an external displsy signal	0	+	1		W	03	00	00	00	*	*	*	*	VSPL	HSPL	EPL	DPL
												0	0	0	0	0	0	1	1
B8	2	Output control	0	+	1		W	FF	F5	00	00	AUTO	CONT	PEV	DCCKEV	STV	CKV	OEV	VCSCOMD
												1	1	1	1	1	1	1	1
												FR	FDON	ASW1	ASW0	VSIG1	VSIG0	DCG	VGAM
												1	1	1	1	0	1	0	1
B9	1	DCCLK and DCEV timing setup	0	+	1		W	24	00	00	00	*	*	DCCKS1	DCCKS0	*	DCEVS2	DCEVS1	DCEVS0
												0	0	1	0	0	1	0	0
BA	1	Display mode setup (1)	0	+	1		W	01	00	00	00	*	*	*	NBW	*	*	*	D8M
												0	0	0	0	0	0	0	1
BB	1	Display mode setup (2)	0	+	1		W	00	00	00	00	*	*	*	*	*	NPC	*	*
												0	0	0	0	0	0	0	0
BC	1	Display mode setup	0	+	1		W	00	00	00	00	SIGCON	*	RAR	RWM1	RWM0	*	DISP1	DISP0
												0	0	0	0	0	0	0	0
BD	1	ASW signal slew rate adjustment	0	+	1		W	02	00	00	00	SRON	*	PBOS	*	*	ASS2	ASS1	ASS0
												0	0	0	0	0	0	1	0
BE	1	Dummy display (whate/black)count setup for QuadData operation	0	+	1		W	00	00	00	00	X2WS3	X2WS2	X2WS1	X2WS0	X2WE3	X2WE2	X2WE1	X2WE0
												0	0	0	0	0	0	0	0
BF	1	Drive system chang control	0	+	1		W	11	00	00	00	*	*	*	VCOMAC	*	*	*	*
												0	0	0	0	0	0	0	0
C0	1	Sleep-out FR count setup(A)	0	+	1		W	11	00	00	00	PTA3	PTA2	PTA1	PTA0	TA3	TA2	TA1	TA0
												0	0	0	1	0	0	0	1
C1	1	Sleep-out FR count setup(B)	0	+	1		W	11	00	00	00	PTB3	PTB2	PTB1	PTB0	TB3	TB2	TB1	TB0
												0	0	0	1	0	0	0	1
C2	1	Sleep-out FR count setup(C)	0	+	1		W	11	00	00	00	PTC3	PTC2	PTC1	PTC0	TC3	TC2	TC1	TC0
												0	0	0	1	0	0	0	1
C3	2	Sleep-in line clock count setup(D)	0	+	1		W	20	40	00	00	PTD7	PTD6	PTD5	PTD4	PTD3	PTD2	PTD1	PTD0
												0	0	1	0	0	0	0	0
												*	TD6	TD5	TD4	TD3	TD2	TD1	TD0
												0	1	0	0	0	0	0	0
C4	2	Sleep-in line clock count setup(E)	0	+	1		W	30	60	00	00	PTE7	PTE6	PTE5	PTE4	PTE3	PTE2	PTE1	PTE0
												0	0	1	1	0	0	0	0
												*	TE6	TE5	TE4	TE3	TE2	TE1	TE0
												0	1	1	0	0	0	0	0
C5	2	Sleep-in line clock count setup(F)	0	+	1		W	10	20	00	00	PTF7	PTF6	PTF5	PTF4	PTF3	PTF2	PTF1	PTF0
												0	0	0	1	0	0	0	0
												*	TF6	TF5	TF4	TF3	TF2	TF1	TF0
												0	0	1	0	0	0	0	0
C6	2	Sleep-in line clock count setup(G)	0	+	1		W	60	C0	00	00	PTG7	PTG6	PTG5	PTG4	PTG3	PTG2	PTG1	PTG0
												0	1	1	0	0	0	0	0
												TG7	TG6	TG5	TG4	TG3	TG2	TG1	TG0
												1	1	0	0	0	0	0	0
C7	2	Gamma 1 fine tuning(1)	0	+	1		W	33	43	00	00	*	PK12	PK11	PK10	*	PK02	PK01	PK00
												0	0	1	1	0	0	1	1
												*	PK32	PK31	PK30	*	PK22	PK21	PK20
												0	1	0	0	0	0	1	1
C8	1	Gamma 1 fine tuning(2)	0	+	1		W	44	00	00	00	*	PK52	PK51	PK50	*	PK42	PK41	PK40
												0	1	0	0	0	1	0	0
C9	2	Gamma 1 inclnation adjustment	0	+	1		W	33	00	00	00	*	PR12	PR11	PR10	*	PR02	PR01	PR00
												0	0	1	1	0	0	1	1
CA	1	Gamma blue offset adjustment	0	+	1		W	00	00	00	00	BLON	BUP2	BUP1	BUP0	*	BOFS2	BOFS1	BOFS0
												0	0	0	0	0	0	0	0

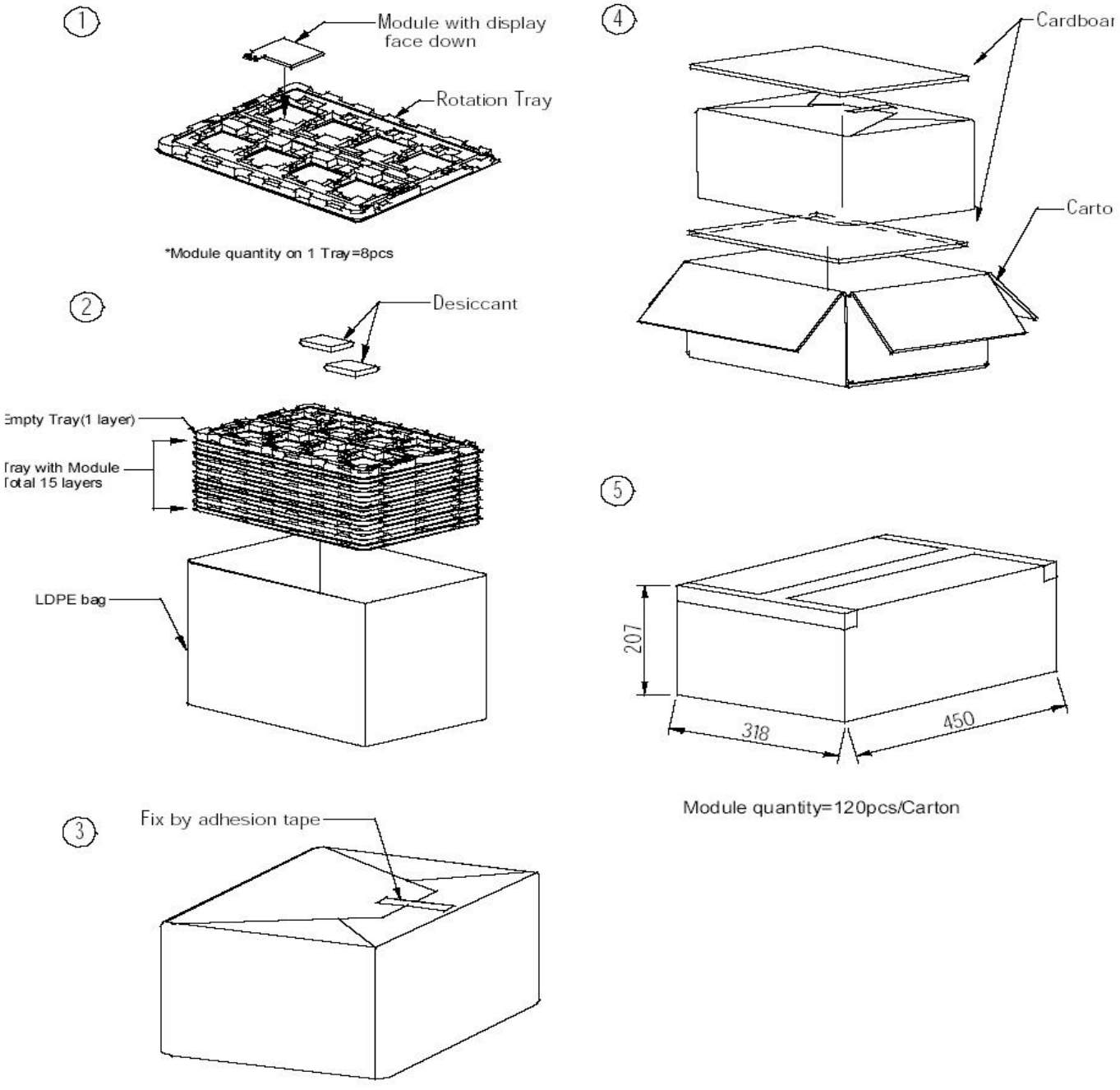
Basic setout command																				
CF	1	Blanking period control (1) [PCLK synchronization:Table1]	0	+	1		W	02	00	00	00	*	*	*	*	*	*	ENAON	THVON
												0	0	0	0	0	0	1	0
D0	2	Blanking period control (2) [PCLK synchronization:Table1]	0	+	1		W	08	04	00	00	TH7	TH6	TH5	TH4	TH3	TH2	TH1	TH0
												0	0	0	0	1	0	0	0
												TV7	TV6	TV5	TV4	TV3	TV2	TV1	TV0
												0	0	0	0	0	1	0	0
D1	1	CKV timing control on/off [PCLK synchronization:Table1]	0	+	1		W	01	00	00	00	*	*	*	*	*	*	*	VKAON
												0	0	0	0	0	0	0	1
D2	2	CKV1,2 timing control [PCLK synchronization:Table1]	0	+	1		W	00	1E	00	00	*	*	CKVS5	CKVS4	CKVS3	CKVS2	CKVS1	CKVS0
												0	0	0	0	0	0	0	0
												*	*	CKVE5	CKVE4	CKVE3	CKVE2	CKVE1	CKVE0
												0	0	0	1	1	1	1	0
D3	2	OVE timing control [PCLK synchronization:Table1]	0	+	1		W	14	28	00	00	*	*	OEVS5	OEVS4	OEVS3	OEVS2	OEVS1	OEVS0
												0	0	0	1	0	0	0	0
												*	*	OEVE5	OEVE4	OEVE3	OEVE2	OEVE1	OEVE0
												0	0	1	0	0	1	0	0
D4	2	ASW timing cotrol (1) [PCLK synchronization:Table1]	0	+	1		W	28	64	00	00	*	*	ASWS5	ASWS4	ASWS3	ASWS2	ASWS1	ASWS0
												0	0	1	0	1	0	0	0
												ASWW7	ASWW6	ASWW5	ASWW4	ASWW3	ASWW2	ASWW1	ASWW0
												0	1	1	0	0	1	0	0
D5	1	ASW timing control (2) [PCLK synchronization:Table1]	0	+	1		W	28	00	00	00	*	*	ASWP5	ASWP4	ASWP3	ASWP2	ASWP1	ASWP0
												0	0	1	0	1	0	0	0
D6	1	Blanking period control (1) [PCLK synchronization:Table2]	0	+	1		W	02	00	00	00	*	*	*	*	*	*	ENAON2	THVON2
												0	0	0	0	0	0	1	0
D7	2	Blanking period control (2) [PCLK synchronization:Table2]	0	+	1		W	08	04	00	00	TH72	TH62	TH52	TH42	TH32	TH22	TH12	TH02
												0	0	0	0	1	0	0	0
												TV72	TV62	TV52	TV42	TV32	TV22	TV12	TV02
												0	0	0	0	0	1	0	0
D8	1	CKV timing control on/off [PCLK synchronization:Table2]	0	+	1		W	01	00	00	00	*	*	*	*	*	*	*	VKVON2
												0	0	0	0	0	0	0	1
D9	2	CKV1,2 timing control [PCLK synchronization:Table2]	0	+	1		W	00	08	00	00	*	*	CKVS52	CKVS42	CKVS32	CKVS22	CKVS12	CKVS02
												0	0	0	0	0	0	0	0
												*	*	CKVE52	CKVE42	CKVE32	CKVE22	CKVE12	CKVE02
												0	0	0	0	1	0	0	0
DA	2	Read ID1	0	+	1		R	74	10	_	_	xx	xx	xx	xx	xx	xx	xx	xx
												0	1	1	1	0	1	0	0
												xx	xx	xx	xx	xx	xx	xx	xx
												0	0	0	1	0	0	0	0
DB to DD		Don't use						00	00	00	00	*	*	*	*	*	*	*	*
DE	2	OEV timing control [PCLK synchronization:Table2]	0	+	1		W	05	0A	00	00	*	*	OEVS52	OEVS42	OEVS32	OEVS22	OEVS12	OEVS02
												0	0	0	0	0	1	0	1
												*	*	OEVE52	OEVE42	OEVE32	OEVE22	OEVE12	OEVE02
												0	0	0	0	1	0	1	0
DF	2	ASW timing control(1) [PCLK synchronization:Table2]	0	+	1		W	0A	19	00	00	*	*	ASWS52	ASWS42	ASWS32	ASWS22	ASWS12	ASWS02
												0	0	0	0	1	0	1	0
												ASWW72	ASWW62	ASWW52	ASWW42	ASWW32	ASWW22	ASWW12	ASWW02
												0	0	0	1	1	0	0	1
E0	1	ASW timing contro(2) [PCLK synchronization:Table2]	0	+	1		W	0A	00	00	00	*	*	ASWP52	ASWP42	ASWP32	ASWP22	ASWP12	ASWP02
												0	0	0	0	1	0	1	0
E1	1	Built-in oscillator on/off	0	+	1		W	00	00	00	00	*	*	*	*	*	*	*	CSCON
												0	0	0	0	0	0	0	0
E2	1	Built-in oscillator frequency division setup	0	+	1		W	00	00	00	00	*	*	*	*	*	OSCR2	OSCR1	OSCR0
												0	0	0	0	0	0	0	0
E3	1	Built-in oscillator clock count setup	0	+	1		W	32	00	00	00	S1H7	S1H6	S1H5	S1H4	S1H3	S1H2	S1H1	S1H0
												0	0	1	1	0	0	1	0
E4	2	CKV timing contorl for using built-in oscillator	0	+	1		W	00	03	00	00	*	*	*	*	SCKS3	SCKS2	SCKS1	SCKS0
												0	0	0	0	0	0	0	0
												*	*	*	*	SCKE3	SCKE2	SCKE1	SCKE0
												0	0	0	0	0	0	1	1
E5	2	OEV timingcontrol for using built-in oscillator	0	+	1		W	02	04	00	00	*	*	*	*	SOES3	SOES2	SOES1	SOES0
												0	0	0	0	0	0	1	0
												*	*	*	*	SEEE3	SEEE2	SEEE1	SEEE0
												0	0	0	0	0	1	0	0
E6	1	DCEV timing control for using built-in oscillator	0	+	1		W	03	00	00	00	*	*	*	*	SEVW3	SEVW2	SEVW1	SEVW0
												0	0	0	0	0	0	1	1
E7	2	ASW timing setup for using built-in oscillator(1)	0	+	1		W	04	0A	00	00	*	*	*	*	SASW3	SASW2	SASW1	SASW0
												0	0	0	0	0	1	0	0

												*	*	*	*	SASWW3	SASWW2	SASWW1	SASWW0
												0	0	0	0	1	0	1	0
E8	1	ASW timing setup for using built-in oscillator(2)	0	+	1		W	04	00	00	00	*	*	*	*	SASWP3	SASWP2	SASWP1	SASWP0
												0	0	0	0	0	1	0	0
E9	1	Booater clock setup for using built-in oscillator	0	+	1		W	10	00	00	00	*	*	PTCKS1	PTCKS0	*	*	*	*
												0	0	0	1	0	0	0	0
EA	2	Vertical blanking count setup for using built-in oscillator	0	+	1		W	10	10	00	00	*	SVBP6	SVBP5	SVBP4	SVBP3	SVBP2	SVBP1	SVBP0
												0	0	0	1	0	0	0	0
												*	SVFP6	SVFP5	SVFP4	SVFP3	SVFP2	SVFP1	SVFP0
												0	0	0	1	0	0	0	
EB	2	Read VCS (B5h) and VCOM (B6h)setting status	0	+	1		W	20	40	00	00	*	*	R1D5	R1D4	R1D3	R1D2	R1D1	R1D0
												0	0	1	0	0	0	0	0
												*	R2D6	R2D5	R2D4	R2D3	R2D2	R2D1	R2D0
												0	1	0	0	0	0	0	0
EC	2	Total number of horizontal clack xycles(1) [PCLK sync.for VGA]	0	+	1		W	01	F0	00	00	*	*	*	*	VHTTL11	VHTTL10	VHTTL9	VHTTL8
												0	0	0	0	0	0	0	1
												VHTTL7	VHTTL6	VHTTL5	VHTTL4	VHTTL3	VHTTL2	VHTTL1	VHTTL0
												1	1	1	1	0	0	0	0
ED	2	Total number of horizontal clack xycles(2) [PCLK sync.for QVGA]	0	+	1		W	00	FF.	00	00	*	*	*	*	*	QHTTL10	QHTTL09	QHTTL08
												0	0	0	0	0	0	0	0
												QHTTL7	QHTTL6	QHTTL5	QHTTL4	QHTTL3	QHTTL2	QHTTL1	QHTTL0
												1	1	1	1	1	1	1	1
EE		Don't use						00	00	00	00	*	*	*	*	*	*	*	*
EF		Don't use						00	00	00	00	*	*	*	*	*	*	*	*

13. Mechanical Drawing



14. Packing Drawing



3.5" Module(TD035STEE1) delivery packing method

(1).Place the module into tray cavity(with display face down).

(2).Stacking the tray with15 layers and with 1 empty tray above the stacking tray unit. and place 2pcs desiccant on the empty tray.

(3).Place the stacking tray unit into the LDPE bag and fixed by adhesive tape.

(4).Place 1pc cardboard inside the carton bottom, then pack the package unit into the carton, and place 1pc cardboard on the package uint.

(5).Sealing the carton with adhesive tape.